Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-14 (canceled).

Claim 15. (new) A method for regulating a threshold and a relative phase of a sampling clock signal with respect to a phase of a binary signal by evaluation of error correction signals, wherein the threshold is associated with an optimum ratio, the method comprising the steps of:

evaluating both a number of 1-bits detected as erroneous and a number of 0-bits detected as erroneous;

adjusting the threshold according to the evaluating step to achieve the optimum ratio of the number of 1-bits detected as erroneous and the number of 0-bits detected as erroneous;

evaluating a number of bits detected as erroneous before a transition between binary states and a number of bits detected as erroneous after a transition between the binary states; and

adjusting the phase of the sampling clock signal such that the number of bits detected as erroneous before and after the transition between the binary states are substantially the same.

Claim 16. (new): A method for regulating a threshold and a relative phase of a sampling clock signal as claimed in claim 15, the method further comprising the steps of:

forming a difference between the number of 1-bits detected as erroneous and the number of 0-bits detected as erroneous; and

converting the difference into an actuating signal for the threshold.

Claim 17. (new): A method for regulating a threshold and a relative phase of a sampling clock signal as claimed in claim 16, the method further comprising the step of setting the threshold, for balanced codes, such that the difference becomes zero.

Claim 18. (new) A system for regulating a decision threshold and a phase of a sampling clock signal of a data regenerator having a decision stage, to which a binary signal and a comparison signal are fed, the system comprising:

a sampling flip-flop having a data input connected to an output of the decision stage;

a controllable clock regenerator which generates a sampling clock signal for the sampling flip-flop;

an error correction device for controlling the controllable clock regenerator; and

a first regulator, wherein a first correction signal, fed into the first regulator from the error correction device, indicates a correction of a 1-bit, and a second correction signal being fed to the first regulator from the error correction device which indicates a correction of a 0-bit, wherein the first regulator separately sums and assesses the first and second correction signals and generates a control signal which determines a magnitude of the comparison signal to adjust the decision threshold to achieve an optimum ratio of the number of 1-bits detected as erroneous and the number of 0-bits detected as erroneous;

a second regulator, wherein a first phase correction signal, fed into the second regulator from the error correction device, indicates a correction of a bit before a signal transition between two binary states, and a second phase corrections signal being fed to the regulator which indicates a correction of a bit after a signal transition between two binary states, the second regulator counting the correction signals and comparing the sums to generate a phase correction signal which generates the phase of sampling clock signal such that at least approximately a same number of correction signals occurs before and after a transition between the binary state.